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Claims

1. Device for processing frequency signals with a power limiter (10), **characterized by the fact**

- that the power limiter (10) has a first signal path (12),
- that the power limiter (10) has a second signal path (14),
- that the first signal path (12) has means (16) for analog signal processing,
- that the second signal path (14) has means (18) for digital signal processing,
- that the means (18) for digital signal processing have means for selective suppression of specific frequency regions, and
- that an output of the first signal path (12) and an output of the second signal path (14) are connected to the means (22) for combining the signals.

2. Device according to Claim 1, **characterized by the fact** that the second signal path (14) has an analog-digital converter (24), and FIR filter (18) and a digital-analog converter (26).

3. Device according to Claim 1 or 2, **characterized by the fact** that a power adjustment, a delay adjustment and an si(x) compensation can be carried out in the FIR filter (18).

4. Device according to one of the preceding claims, **characterized by the fact** that the FIR filter (18) has steep filter flanks.

5. Device according to one of the preceding claims, **characterized by the fact** that the FIR filter (18) operates at the scanning rate of the converters (24, 26).

6. Device according to one of the preceding claims, **characterized by the fact** that the FIR filter (18) is implemented by means of a filter bank (28).

7. Device according to one of the preceding claims, **characterized by the fact** that the first signal path (12) has an analog delay element (16).

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8. Device according to one of the preceding claims, **characterized by the fact** that the analog delay element (16) has a constant group delay.

9. Device according to one of the preceding claims, **characterized by the fact** that the constant group delay corresponds to the total delay of the converters (24, 26) and of the FIR filter (18).

10. Device according to one of the preceding claims, **characterized by the fact** that the means for combining the signals have an analog adder (22).

11. Device according to one of the preceding claims, **characterized by the fact** that the output signal of the analog adder (22) can be fed to an analog-digital converter module (46).

12. Device according to one of the preceding claims, **characterized by the fact** that the input frequency signal can be fed to means (22) for analog preprocessing.

13. Device according to one of the preceding claims, **characterized by the fact** that a calibration signal (58) can be fed to the input frequency signal.

14. Device according to one of the preceding claims, **characterized by the fact** that a third signal path (32) is provided, which implements an equivalent channel digitally, in which a scanning rate reduction occurs, the third signal path (32) having a complex mixer (34) and an FIR filter (76, 78).

15. Device according to one of the preceding claims, **characterized by the fact** that the output signal of the analog-digital converter module (46) can be fed to a fourth signal path (38), in which a scanning rate reduction occurs, the fourth signal path (38) having a complex mixer (70) and an FIR filter (72).

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16. Device according to one of the preceding claims, **characterized by the fact** that an output of the third signal path (32) and an output of the fourth signal path (38) are connected to means (44) for combination of signals.

17. Device according to one of the preceding claims, **characterized by the fact** that the output signal of the analog-digital converter module (46) can be fed back to at least one FIR filter (62, 78) via a calibration unit (48).

18. Device according to one of the preceding claims, **characterized by the fact** that the output signal of the analog-digital converter module (46) can be fed back to an adjustable amplifier (50) of the analog-digital converter module (46) via a calibration unit (48).

19. Method for processing frequency signals, in which a power is limited, **characterized by the fact**

- that the frequency signal is fed to a first signal path (12),
- that the frequency signal is fed to a second signal path (14),
- that an analog signal processing occurs in the first signal path (12),
- that a digital signal processing occurs in the second signal path (14),
- that specific frequency regions are selectively suppressed in the digital signal processing, and
- that a signal resulting from analog signal processing is combined with a signal resulting from analog signal processing [sic].

20. Method according to Claim 19, **characterized by the fact** that a signal is digitized in the second signal path (14), the digitized signal is fed to an FIR filter (18) and the filtered signal is fed to the digital-analog converter (26).

21. Method according to Claim 19 or 20, **characterized by the fact** that a power adjustment, a delay adjustment and an si(x) compensation are carried out in the FIR filter.

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22. Method according to one of the Claims 19 to 21, **characterized by the fact** that the FIR filter (18) is operated at the scanning rate of the converters (24, 26).

23. Method according to one of the Claims 19 to 22, **characterized by the fact** that a signal is delayed in the first signal path (32) to an extent that corresponds to the total delay of the converters (24, 26) and of the FIR filter (18, 62) of the second signal path (14).

24. Method according to one of the Claims 19 to 23, **characterized by the fact** that the signal resulting from digital signal processing is subtracted from the signal resulting from analog signal processing.

25. Method according to one of the Claims 19 to 24, **characterized by the fact** that the signal resulting from subtraction is fed to an analog-digital converter module (46).

26. Method according to one of the Claims 18 to 25, **characterized by the fact** that the input frequency signal is preprocessed in analog fashion.

27. Method according to one of the Claims 19 to 26, **characterized by the fact** that a calibration signal (58) is fed to the input frequency signal.

28. Method according to one of the Claims 19 to 27, **characterized by the fact** that an output signal of an analog-digital converter (24) in the second signal path (14) is fed to a third signal path (32) that implements an equivalent channel with a complex mixer (68) and an FIR filter (76, 78), in which the scanning rate is reduced.

29. Method according to one of the Claims 19 to 28, **characterized by the fact** that the output signal of the analog-digital converter module (46) is fed to a fourth signal path (38) having a complex mixer (74) and an FIR filter (80), in which the scanning rate is reduced.

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30. Method according to one of the Claims 19 to 29, **characterized by the fact** that an output signal of the third signal path (32) is combined with the output signal of the fourth signal path (38).

31. Method according to one of the Claims 19 to 30, **characterized by the fact** that the output signal of the analog-digital converter module (46) is fed back to at least one FIR filter (62, 78) via a calibration unit (48).

32. Method according to one of the Claims 19 to 31, **characterized by the fact** that the output signal of the analog-digital converter module (46) is fed back to an adjustable amplifier (50) of the analog-digital converter module (46) via a calibration unit (48).

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